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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
LINDINGER, MICHAEL L

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 11/20/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/703,344	BERSTIS ET AL.	
	Examiner	Art Unit	
	Michael L. Lindinger	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-50 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-50 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on 10 September 2002 is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to Claim 1-29 have been considered but are moot in view of the new ground(s) of rejection.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

1. Claim 1 is provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claim 1 of copending Application No. 09/703,340, 09/703,334, and 09/703,335. Although the conflicting claims are not identical, they are not patentably distinct from each other because discloses a time cell, which experiences a transition of states after a programming

(charging) operation, detections means for detecting a value within a charge storage element, which is located within the time cell.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Drawings

1. The corrected or substitute drawings were received on September 10, 2002. These drawings are acceptable.

Sp cification

1. The corrected or substitute Specification was received on September 10, 2002. The Specification is acceptable.

2. The Applicant has explained the term "programming operation" sufficiently; therefore, the Examiner is withdrawing the objection to the Specification language in regards to this matter.

Claim Rejections - 35 USC § 112

1. The Applicant has both amended and provided an additional explanation to the Examiner regarding the Claims to more clearly define the Claimed "reading means", therefore, the Examiner's rejection under 112 2nd paragraph is withdrawn.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-17 and 22-50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakaki U.S. Patent No. 5,500,834 in view of Feddeler U.S. Patent No. 5,323,066 in further view of the Admitted Prior Art. Regarding Claims 1-2, 22-27, 30-38, 46-47, and 49-50, Sakaki teaches a horological device for measuring the time lapse after a turn off of a power source, wherein a capacitor is charged when power supplied to the system is turned on, wherein the capacitor is discharged when the power is disconnected, wherein the voltage of the capacitor is read (by reading/coupling means) and recorded by a processor, which then interprets and converts information appropriately when the power is turned, wherein the capacitor's value is also read and recorded when the power is turned off, wherein a corresponding time lapse is recorded, wherein inherently this teaches a time detection unit for processing a time request to generate a time response after reading the capacitor's value, thereby measuring the electrostatic charge of the capacitor, wherein the above mentioned elements combine to form claimed time cell, wherein the capacitor (Col. 1, lines 10+; Col. 2, lines 25+; Col. 3, lines 1+; Col. 4, lines 5+; FIG. 1). Sakaki does not teach a horological device

comprising a floating gate in a floating gate field effect transistor (FGFET), explicit time determining means, or the length of a predetermined time period varies with an initial condition of the time cell after the charging operation, wherein the initial condition is determined by an initial electrical potential of the charge storage element. Feddeler teaches a data acquisition means that comprising a capacitor that is replaced with a floating gate in a floating gate field effect transistor (FGFET) (Col. 4, lines 12+; FIG. 5). Neither Sakaki nor Feddeler explicitly teach the electrical components claimed. The Admitted Prior Art teaches a device comprising all of the structural features shown in FIGURE 1A: a semiconductor substrate 102, a source region 104, a drain region 106, a channel region 122 between the source region and the drain region, a control gate 116, a floating gate 118 between the control gate and the channel region, wherein the floating gate behaves as a charge stored element in a floating gate field effect transistor (FGFET), wherein an internal medium is provided within the charged storage element to receive programming operations, hereafter referred as charging operations, an insulating medium 120 surrounding the internal medium, wherein the insulating medium has a tunneling region for discharging an electrostatic charge, wherein said insulating medium has physical properties which affect the rate of discharge in a discharge process, wherein one of these physical properties is the thickness of the insulating medium. The discharge process is a non-linear Fowler-Nordheim tunneling process and the charging process is a channel hot electron injection process, which comprising a charge injector for injecting said charge into charge storage element, further comprises a programming unit, hereto referred to as a charging unit for charging the charge

storage element. It would have been obvious to a person skilled in the art at the time of the invention to not only adapt the Sakaki reference and include a floating gate in a floating gate field effect transistor (FGFET) in place of a capacitor in order to further insulate the charge element that is being charged and discharged, but to recognize that any capacitive timing device must inherently possesses the structure and means to read and interpret data as to whether or not a predetermined time period has elapsed in order to verify the time at which to charge the time cell again, as well as to recognize the length of the predetermined time period may be altered by varying the insulating medium after the charging operation, wherein by altering this thickness, initial electrical potential of the charge storage element is directly impacted, and to further recognize that by including the structural features of the Admitted Prior Art, the rate of electrostatic discharge may controlled more easily. Sakaki teaches all of the necessary structure, the methods of charging a charge storage element within controlling electrostatic discharge during and after discharging and charging states of a time cell in order to gain measurement of the elapsed time of the system and the corresponding charging and read operation steps needed to initialize and process the information of the apparatus are inherently possessed within said structure.

Regarding Claims 3-5, the combination of the Sakaki and Feddeler references coupled with the Admitted Prior Art as explained above teaches a time cell, which has the ability of a conventional RC timer to measure electrostatic discharge in order to measure elapsed time. The combination does not explicitly teach an array of time cells, or the

time periods of the time cells in the array of time cell. It would have been obvious to a person skilled in the art at the time of the invention to provide an array of time cells comprising individual time periods whose values maybe the same or different, since it has been held that the mere duplication of parts for a multiplied effect, in the instant an array of time cells for various time measurements, is an obvious improvement (*In re Harza*, 274 F.2d 669, 671, 124 USPQ 378, 380 (CCPA 1960)).

Regarding Claims 6-7 and 28-29, the combination of the Sakaki, Feddeler references coupled with the Admitted Prior Art as explained above teaches a time cell, which has the ability of a conventional RC timer to measure electrostatic discharge in order to measure elapsed time. The combination does not explicitly comprise a time cell interface unit, programming request unit, or a status-generating unit for initializing or setting one or more time cells, as well as generating status from the time cells. It would have been obvious to a person skilled in the art at the time of the invention to recognize that any capacitive timing device must inherently possesses the structure and means to charge/discharge time cells, as well as the ability to determine during the charging process whether the cells were successfully charged or not. By including a time cell interface unit and a programming request unit, existing initialization structure of a typical RC timer is applied to the specific invention.

Regarding Claims 8-12, 31-35, and 42-43, the modified combination of the Sakaki and Feddeler references inherently possess the methods of controlling electrostatic

discharge during and after discharging and charging states of a time cell in order to gain measurement of the elapsed time of the system and the corresponding charging and read operation steps needed to initialize and process the information of the apparatus. It would be obvious to a person skilled in the art at the time of the invention to recognize that because the modified combination of the Sakaki and Feddeler references form the structure of the inventive entity claimed, the methods needed to construct, charge, and read the components and data contained and produced are inherently possessed by the structure.

Regarding Claims 13-17 and 44-45, it would be obvious to a person skilled in the art at the time of the invention to construct a computer program to perform the method steps of Claims. It is well known in the art to build a computer program on a computer readable medium such as a floppy disk for easy insertion and data recall during use on a computer.

Regarding Claim 39, the modified combination of the Sakaki and Feddeler references in view of the Admitted Prior Art teaches a time cell comprising a tunneling region, which has the ability of a conventional RC timer to measure electrostatic discharge in order to measure elapsed time, wherein the details of the combination are explained above. The combination does not explicitly teach the thickness of the tunneling region being less than 7 nanometers. It would be obvious to a person skilled in the art to recognize that reducing the thickness of the tunneling region increases electron flow, thereby

increasing the ability to control electrostatic discharge. A typical RC timer comprises capacitive plates whose distance relative to one another, which can comprise of air, insulating material or any non-conductive material, can be varied in order to increase or decrease the amount of electrons that pass through the gap during electrostatic discharge, therefore controlling the electrostatic discharge. By applying a typical RC timer characteristics regarding thickness of the insulating region, the electrostatic discharge of a charge storage element can be controlled.

Regarding Claims 40-41, the Admitted Prior Art teaches the structure as described in detail above, as well as the ability to measure threshold voltage of the floating gate field effect transistor at a predetermined time after charging operations are performed on the floating gate (FIG. 1C-1J).

Regarding Claim 48, the combination of the Sakaki and Feddeler references teaches a time cell, which has the ability of a conventional RC timer to measure electrostatic discharge in order to measure elapsed time. The Sakaki/Feddeler combination does not explicitly teach an article of manufacturing comprising a smart card. It would be obvious to a person skilled in the art at the time of the invention to adapt a smart card to include a charge storage device, e.g. an RC timer device in order to to measure elapsed time of a charged storage element with a smart card in order to calculate the elapsed time memory has been stored on a smart card. Any capacitive timing device possesses memory and means to store and read the memory and by applying this concept of

measuring electrostatic discharge to calculate memory, a user may read the elapsed time a portion of memory that has been stored on the smart card and recharge or update the memory before it is erased.

2. Claims 18-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakaki U.S. Patent No. 5,500,834 in view of Suzuki U.S. Patent No. 4,442,363. Regarding Claim 18-19, Sakaki teaches a horological device for measuring the time lapse after a turn off of a power source, wherein a capacitor is charged when power supplied to the system is turned on, wherein the capacitor is discharged when the power is disconnected, wherein the voltage of the capacitor is read (by reading/coupling means) and recorded by a processor, which then interprets and converts information appropriately when the power is turned, wherein the capacitor's value is also read and recorded when the power is turned off, wherein a corresponding time lapse is recorded, wherein inherently this teaches a time detection unit for processing a time request to generate a time response after reading the capacitor's value, thereby measuring the electrostatic charge of the capacitor, wherein the above mentioned elements combine to form claimed time cell, wherein the capacitor (Col. 1, lines 10+; Col. 2, lines 25+; Col. 3, lines 1+; Col. 4, lines 5+; FIG. 1). Sakaki does not explicitly teach the specific states or modes the capacitor experiences during the charging and discharging process. Suzuki teaches a conventional RC timer, wherein a typical RC timer experiences different states or modes, which are achieved in the timer's life in respect to charging and discharging, wherein in a first state or mode, the timer is discharging, in a second

state or mode, the timer is charging, in a third state or mode, the timer is fully charged, in a fourth state or mode, the timer is discharging, and finally, in a fifth state or mode, the timer is fully discharged (Col. 1, lines 12+). Suzuki does not teach a length of a predetermined time period varying after the charging operation. It would be obvious to a person skilled in the art to adapt the Sakaki reference to provide specific states the capacitor enters and leaves in order to better read the values associated at a given time. One skilled in the art would also recognize that any changes to an initial condition will only be visible when the charge storage element has completed the charging process and data can be acquired regarding threshold voltage versus time.

Regarding Claim 20, Suzuki teaches a conventional RC timer, wherein a typical RC timer experiences different states or modes, which are achieved during the course of operation of the timer in respect to charging and discharging, wherein in a first state or mode, the timer is completely discharged, in a second state or mode, the timer is charging, in a third state or mode, the timer is discharging (Col. 1, lines 12+).

Regarding Claim 21, Suzuki teachings inherently possess the methods of transitioning within a typical RC timer between different states or modes, which are achieved during the course of operation of the timer in respect to charging and discharging, wherein in a first state or mode, the timer is completely discharged, in a second state or mode, the timer is charging, in a third state or mode, the timer is discharging (Col. 1, lines 12+). Suzuki does not explicitly teach detecting a state of the charge storage element to

determine an elapsed time. It would be obvious to a person skilled in the art to recognize a typical RC timer possesses a circuit used in order to detect the particular state of the charge storage element to determine elapsed time. By possessing a circuit enabled to read a specific state of a charge storage element, an RC timer can measure the amount of electrostatic discharge, thereby providing means to calculate elapsed time.

Prior Art

1. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Ishibashi U.S. Patent No. 5,374,904 discloses a phase-locked loop circuit having adjustable reference clock signal frequency and filter capacitance compensation.
- Ma U.S. Patent No. 6,067,244 discloses a ferroelectric dynamic random access memory, wherein an FE transistor replaces a capacitor.
- Begin U.S. Patent No. 4,995,019 discloses a time period measuring apparatus wherein time measure is achieved by utilizing a time variable interpose, which comprises components that correspond to an RC circuit.
- Curtis U.S. Patent No. 5,195,061 discloses a practice timer for measuring elapsed time during an activity comprising a variable time constant RC circuit.
- Takeda U.S. Patent No. Re. 35,043 discloses a self-charging electronic timepiece comprising a time constant RC circuit.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael L. Lindinger whose telephone number is (703) 305-0618. The examiner can normally be reached on Monday-Thursday (7:30-6).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Martin can be reached on (703) 308-3121. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7318 for regular communications and (703) 746-7318 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Michael L. Lindinger
Patent Examiner
Art Unit 2841

MLL
November 15, 2002

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